



CEZ2R04A

## N-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

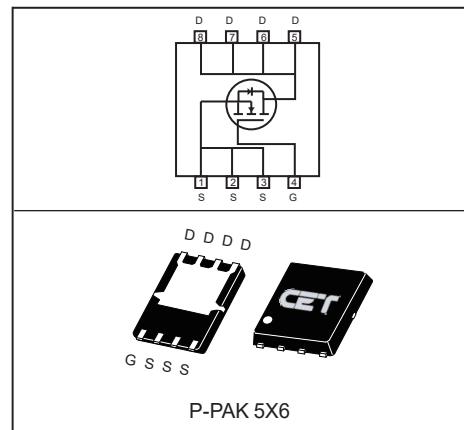
## FEATURES

- High power and current handing capability.
- Reliable and rugged.
- Pb-free lead plating ; RoHS compliant.
- Halogen Free.
- Surface mount Package.

## APPLICATIONS

- DC-DC Conversion.
- Or-ing.
- BLDC motor drive.
- Load Switch.

$V_{DSS}$	$R_{DS(ON)\text{ typ}} @ V_{GS}$	$I_D$
40V	1.8m $\Omega$ @ $V_{GS} = 10V$	124A

ABSOLUTE MAXIMUM RATINGS  $T_C = 25^\circ\text{C}$  unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D @ R_{JC}$	$T_C = 25^\circ\text{C}$	A
		$T_C = 70^\circ\text{C}$	A
	$I_D @ R_{JA}$	$T_A = 25^\circ\text{C}$	A
		$T_A = 70^\circ\text{C}$	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM} @ R_{JC}$	$T_C = 25^\circ\text{C}$	A
		$T_A = 25^\circ\text{C}$	A
Maximum Power Dissipation	$P_D$	57	W
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

## Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{JC}$	2.2	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{JA}$	20	$^\circ\text{C}/\text{W}$

This is preliminary information on a new product in development now  
Details are subject to change without notice .

2025.Aug

<http://www.cet-mos.com>



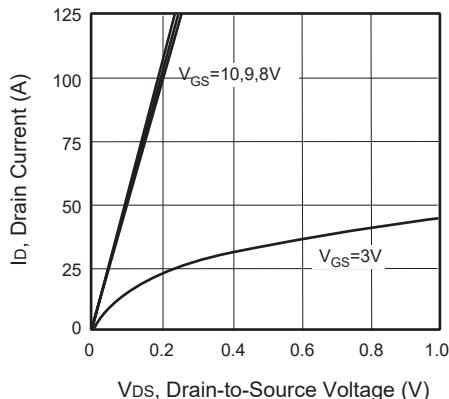
CEZ2R04A

**Electrical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted

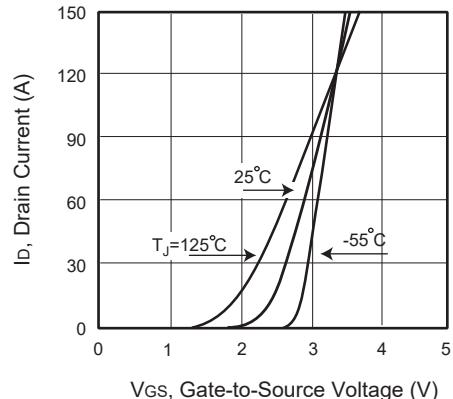
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	40			V
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}} = 40\text{V}, V_{\text{GS}} = 0\text{V}$		1		$\mu\text{A}$
Gate Body Leakage Current, Forward	$I_{\text{GSSF}}$	$V_{\text{GS}} = 20\text{V}, V_{\text{DS}} = 0\text{V}$		100		nA
Gate Body Leakage Current, Reverse	$I_{\text{GSSR}}$	$V_{\text{GS}} = -20\text{V}, V_{\text{DS}} = 0\text{V}$		-100		nA
<b>On Characteristics</b> <sup>b</sup>						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 250\mu\text{A}$	1		3	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_D = 20\text{A}$		1.8	2.3	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5\text{V}, I_D = 20\text{A}$		2.7	3.5	$\text{m}\Omega$
Gate input resistance	$R_g$	f=1MHz,open Drain		0.8		$\Omega$
<b>Dynamic Characteristics</b> <sup>c</sup>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}} = 15\text{V}, V_{\text{GS}} = 0\text{V}, f = 1.0 \text{ MHz}$		3250		pF
Output Capacitance	$C_{\text{oss}}$			640		pF
Reverse Transfer Capacitance	$C_{\text{rss}}$			635		pF
<b>Switching Characteristics</b> <sup>c</sup>						
Turn-On Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 15\text{V}, I_D = 1\text{A}, V_{\text{GS}} = 10\text{V}, R_{\text{GEN}} = 6\Omega$		28		ns
Turn-On Rise Time	$t_r$			24		ns
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$			80		ns
Turn-Off Fall Time	$t_f$			37		ns
Total Gate Charge	$Q_g$	$V_{\text{DS}} = 15\text{V}, I_D = 16\text{A}, V_{\text{GS}} = 4.5\text{V}$		37		nC
Gate-Source Charge	$Q_{\text{gs}}$			8		nC
Gate-Drain Charge	$Q_{\text{gd}}$			26		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				47	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{\text{SD}}$	$V_{\text{GS}} = 0\text{V}, I_S = 20\text{A}$			1.2	V

## Notes :

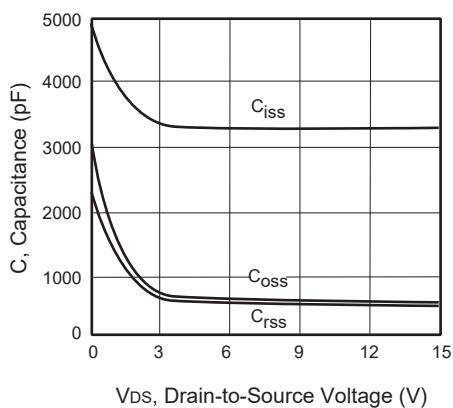
- a.Repetitive Rating : Pulse width limited by maximum junction temperature.
- b.Pulse Test : Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- c.Guaranteed by design, not subject to production testing.



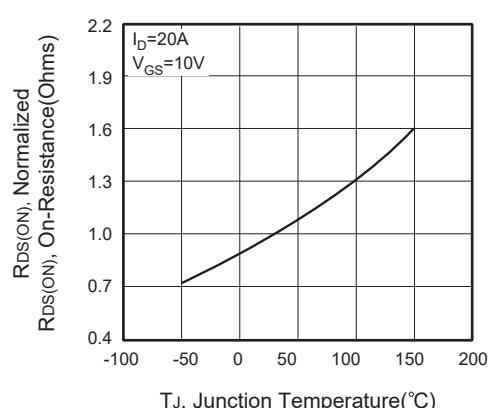
**Figure 1. Output Characteristics**



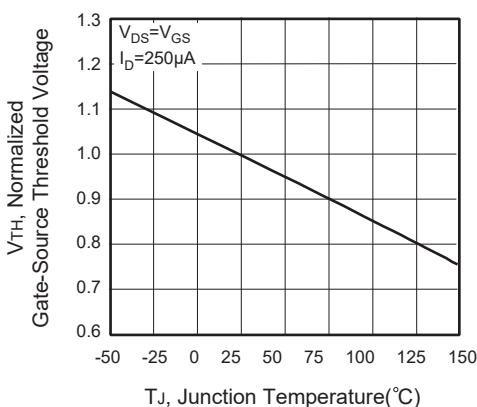
**Figure 2. Transfer Characteristics**



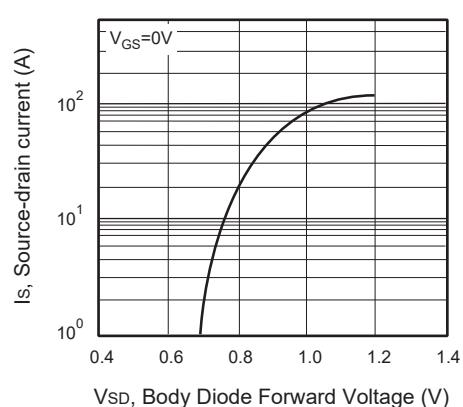
**Figure 3. Capacitance**



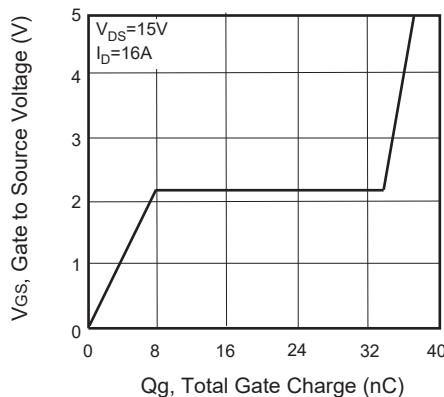
**Figure 4. On-Resistance Variation with Temperature**



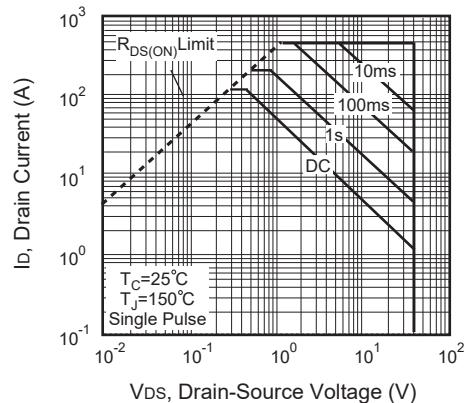
**Figure 5. Gate Threshold Variation with Temperature**



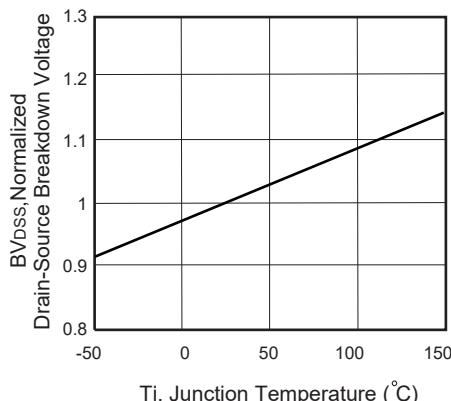
**Figure 6. Body Diode Forward Voltage Variation with Source Current**



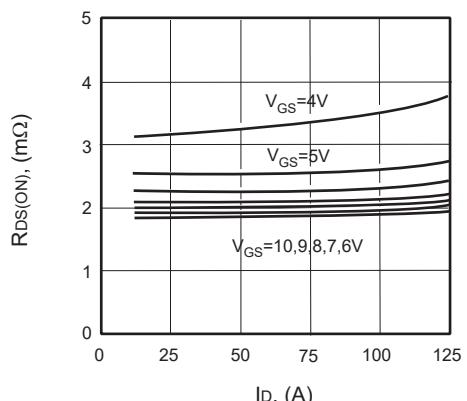
**Figure 7. Gate Charge**



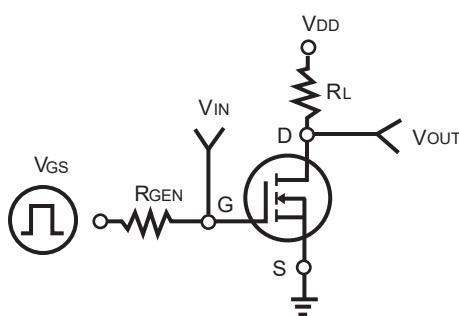
**Figure 8. Maximum Safe Operating Area**



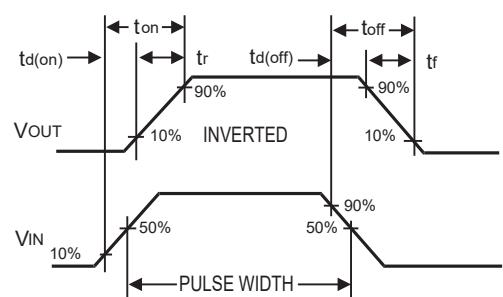
**Figure 9. Breakdown Voltage Variation VS Temperature**



**Figure 10. On-Resistance vs. Drain Current**



**Figure 11. Switching Test Circuit**



**Figure 12. Switching Waveforms**

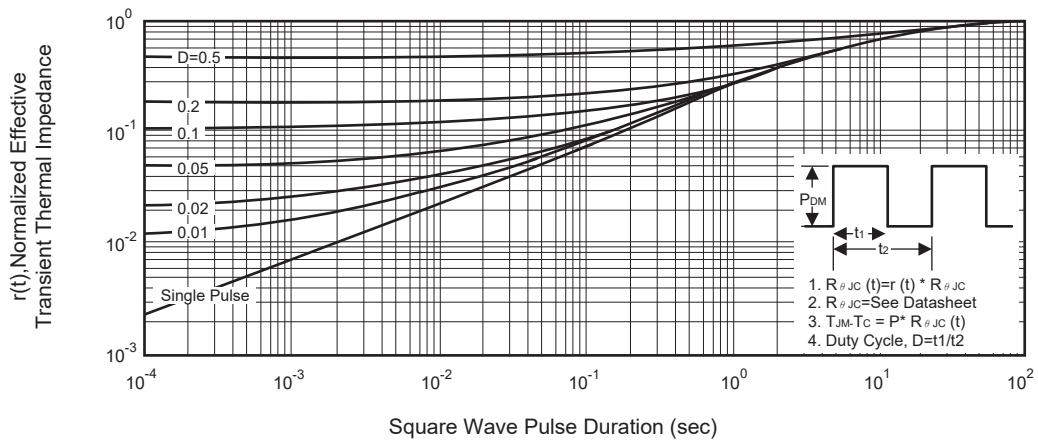
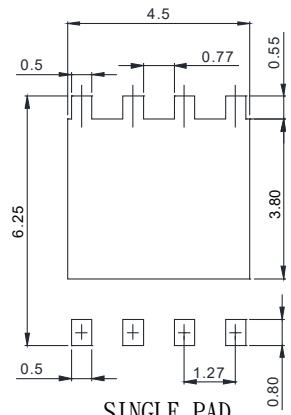
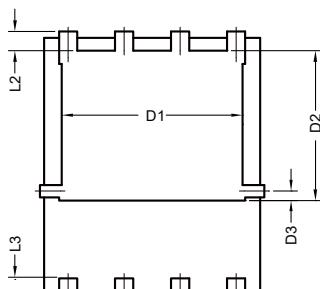
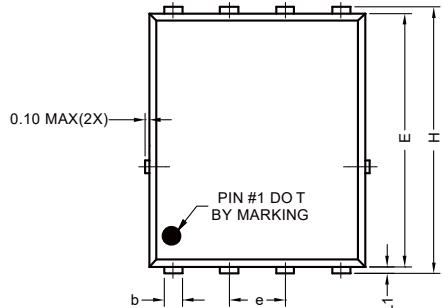
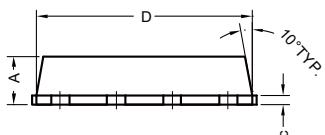


Figure 13 Normalized Thermal Transient Impedance Curve

**P-PAK5X6 產品外觀尺寸圖 (Product Outline Dimension)**
**SINGLE PAD 尺寸圖**


RECOMMENDED LAND PATTERN



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.800	1.170	0.031	0.046
b	0.340	0.490	0.013	0.019
c	0.20	0.34	0.008	0.013
D	4.800	5.100	0.009	0.011
D1	3.800	4.200	0.150	0.165
D2	3.180	3.78	0.125	0.149
D3	0.150	0.360	0.006	0.142
E	5.650	5.900	0.222	0.232
e	1.270 TYP		0.050 TYP	
H	5.900	6.150	0.232	0.242
L1	0.050	0.250	0.002	0.010
L2	0.380	0.620	0.015	0.024
L3	0.380	0.75	0.015	0.030